Day : Wednesday

PALM INTRANET

Date: 3/23/2005
Time: 09:43:33

Inventor Name Search Result

Your Search was:

Last Name = SCHLANGER
First Name = STEVEN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10897325	Not Issued	020	07/22/2004	DEVICES AND METHODS FOR PROGRAMMING MICROCONTROLLERS	SCHLANGER, STEVEN
10921790	Not Issued	020	08/18/2004	DEVICES AND METHODS FOR COMMUNICATING WITH A MICROCONTROLLER	SCHLANGER, STEVEN
07014705	4779007	150	02/13/1987	UNINTERRUPTED POWER SUPPLY SYSTEM	SCHLANGER, STEVEN E.
07026626	Not Issued	161	03/17/1987	HIGH EFFICIENCY CONVERTER CIRCUIT	SCHLANGER, STEVEN E.
09827273	Not Issued	071	04/05/2001	EVENT DETECTION WITH A DIGITAL PROCESSOR	SCHLANGER, STEVEN ERIC
09862079	Not Issued	161	05/21/2001	INFRARED ENCODER/DECODER HAVING HARDWARE AND SOFTWARE DATA RATE SELECTION	SCHLANGER, STEVEN ERIC
09862080	Not Issued	030	05/21/2001	FUNCTIONAL PATHWAY CONFIGURATION AT A SYSTEM/IC INTERFACE	SCHLANGER, STEVEN ERIC
09866236	Not Issued	030	05/25/2001	FUNCTIONAL PATHWAY CONFIGURATION AT A SYSTEM/IC INTERFACE	SCHLANGER, STEVEN ERIC
09866991	6810435	150	05/29/2001	PROGRAMMABLE IDENTIFICATION IN A COMMUNICATIONS CONTROLLER	SCHLANGER, STEVEN ERIC
07981279	Not Issued	161	11/25/1992	CD-ROM INTERFACE APPARATUS AND METHOD	SCHLANGER, STEVEN ERIC

Inventor Search Completed: No Records to Display.

Search Another: Inventor

Last Name: schlanger

First Name: steven

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Date: 3/23/2005
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Inventor Name Search Result

Your Search was:

Last Name = YACH
First Name = RANDY

Application#	Patent#	Status	Date Filed	Title	Inventor Name
08671011	5870409	250	06/28/1996	METHOD AND APPARATUS FOR TESTING A RELATIVELY SLOW SPEED COMPONENT OF AN INTERGRATED CIRCUIT HAVING MIXED SLOW SPEED AND HIGH SPEED COMPONENTS	YACH, RANDY
09280112	6708268	150	03/26/1999	MICROCONTROLLER INSTRUCTION SET	YACH, RANDY
09705723	Not Issued	161	11/06/2000	METHOD AND APPARATUS FOR PROVIDING A RAMPED HIGH VOLTAGE	YACH, RANDY
09957283	Not Issued	071	09/20/2001	REGISTER BANK	YACH, RANDY
10751210	Not Issued	030	12/31/2003	MICROCONTROLLER INSTRUCTION SET	YACH, RANDY
10796771	Not Issued	030	03/09/2004	MICROCONTROLLER INSTRUCTION SET	YACH, RANDY
60564828	Not Issued	020	04/23/2004	DYNAMIC CONFIGURATION OF AN RF TRANSPONDER	YACH, RANDY
60564829	Not Issued	020	04/23/2004	PROGRAMMABLE WAKE-UP FILTER FOR RADIO FREQUENCY TRANSPONDER	YACH, RANDY
09513427	6198691	150	02/25/2000	FORCE PAGE PAGING SCHEME FOR MICROCONTROLLERS OF VARIOUS SIZES USING DATA RANDOM ACCESS MEMORY	YACH, RANDY L.
09587303	Not Issued	161	06/05/2000	DATA POINTER FOR OUTPUTTING INDIRECT ADDRESSING MODE ADDRESSES WITHIN A SINGLE CYCLE ANDMETHOD THEREFOR	YACH, RANDY L.
09666551	Not Issued	161	09/21/2000	APPARATUS FOR ACTIVE HIGH SPEED-LOW POWER ANALOG VOLTAGE DRIVE	YACH, RANDY L.
09684006	Not Issued	161	10/06/2000	TIME DELAY CIRCUIT WHICH IS VOLTAGE INDEPENDENT	YACH, RANDY L.
09707091	Not Issued	161	11/06/2000	CONFIGURABLE MIXED ANALOG AND DIGITAL MODE CONTROLLER SYSTEM	YACH, RANDY L.
09756304	6321319	150	01/08/2001	A COMPUTER SYSTEM FOR ALLOWING A TWO WORD JUMP INSTRUCTION TO BE EXECUTED IN THE SAME NUMBER OF CYCLES AS A SINGLE WORD JUMP INSTRUCTION	YACH, RANDY L.
09799320	Not	168	03/05/2001	FORCE PAGE PAGING SCHEME FOR	YACH, RANDY L.

	Issued			MICROCONTROLLERS OF VARIOUS SIZES USING DATA RANDOM ACCESS MEMORY	
09827273	Not Issued	071	04/05/2001	EVENT DETECTION WITH A DIGITAL PROCESSOR	YACH, RANDY L.
09846018	6593639	150	04/30/2001	IMPROVED LAYOUT TECHNIQUE FOR A CAPACITOR ARRAY USING CONTINUOUS UPPER ELECTRODES	YACH, RANDY L.
09972563	6504191	150	10/08/2001	INDEPENDENTLY PROGRAMMABLE MEMORY SEGMENTS WITHIN A PMOS ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY ARRAY ACHIEVED BY N-WELL SEPARATION AND METHOD THEREFOR	YACH, RANDY L.
10787387	Not Issued	030	02/26/2004	LOW CAPACITANCE ESD-PROTECTION STRUCTURE UNDER A BOND PAD	YACH, RANDY L.
10809659	Not Issued	030	03/25/2004	HIGH VOLTAGE ESD-PROTECTION STRUCTURE	YACH, RANDY L.
60513910	Not Issued	159	10/23/2003	MICROCONTROLLER INSTRUCTION SET	YACH, RANDY L.
07790962	Not Issued	166	11/12/1991	MICROCONTROLLER POWER-UP DELAY	YACH, RANDY L.
08238121	5454114	250	04/04/1994	MICROCONTROLLER POWER-UP DELAY	YACH, RANDY L.
08368919	5606511	150	01/05/1995	MICROCONTROLLER WITH BROWNOUT DETECTION	YACH, RANDY L.
08508332	5587866	250	07/27/1995	POWER-ON RESET CIRCUIT	YACH, RANDY L.
08554741	5737548	150	11/07/1995	RISC-BASED MICROCONTROLLER WITH PERIPHERAL FUNCTION ADDED TO A SPLIT DATA BUS	YACH, RANDY L.
08666993	Not Issued	161	06/19/1996	REMOTE KEYLESS ENTRY DEVICE	YACH, RANDY L.
08723924	5805507	150	10/01/1996	VOLTAGE REFERENCE GENERATOR FOR EPROM MEMORY ARRAY	YACH, RANDY L.
08723925	Not Issued	161	10/01/1996	HIGH VOLTAGE LEVEL SHIFTING CMOS BUFFER	YACH, RANDY L.
08723926	5703809	150	10/01/1996	OVERCHARGE/DISCHARGE VOLTAGE REGULATOR FOR EPROM MEMORY ARRAY	YACH, RANDY L.
08723927	5812456	250	10/01/1996	SWITCHED GROUND READ FOR EPROM MEMORY ARRAY	YACH, RANDY L.
08779907	5889829	150	01/07/1997	PHASE LOCKED LOOP WITH IMPROVED LOCK TIME AND STABILITY	YACH, RANDY L.
08866359	5815445	250	05/30/1997	VOLTAGE REGULATOR FOR CLAMPING A ROW VOLTAGE OF A MEMORY CELL	YACH, RANDY L.
08871340	5835410	150	06/09/1997	SELF TIMED PRECHARGE SENSE AMPLIFIER FOR A MEMORY ARRAY	YACH, RANDY L.
08887876	6055211	150	07/03/1997	FORCE PAGE ZERO PAGING SCHEME FOR MICROCONTROLLERS USING DATA RANDOM ACCESS MEMORY	YACH, RANDY L.
08891348	5793684	150	07/10/1997	MEMORY DEVICE HAVING SELECTABLE	YACH, RANDY L.

				REDUNDANCY FOR HIGH ENDURANCE AND RELIABILITY AND METHOD THEREFOR	
08958940	6243798	150	10/28/1997	A COMPUTER SYSTEM FOR ALLOWING A TWO WORD JUMP INSTRUCTION TO BE EXECUTED IN THE SAME NUMBER OF CYCLES AS SINGLE WORD JUMP INSTRUCTION	YACH, RANDY L.
08959559	6098160	150	10/28/1997	DATA POINTER FOR OUTPUTTING INDIRECT ADDRESSING MODE ADDRESSES WITHIN A SINGLE CYCLE AND METHOD THEREFOR	YACH, RANDY L.
09014458	6122205	150	01/28/1998	VOLTAGE REGULATOR AND BOOSTING CIRCUIT FOR READING A MEMORY CELL AT LOW VOLTAGE LEVELS	YACH, RANDY L.
09138714	6150864	150	08/24/1998	TIME DELAY CIRCUIT WHICH IS VOLTAGE INDEPENDENT	YACH, RANDY L.
09200542	6208500	150	11/25/1998	IMPROVED HIGH QUALITY FACTOR CAPACITOR	YACH, RANDY L.
09221634	6225678	150	12/23/1998	LAYOUT TECHNIQUE FOR A MATCHING CAPACITOR ARRAY USING A CONTINUOUS TOP ELECTRODE	YACH, RANDY L.
09272675	6300183	150	03/19/1999	INDEPENDENTLY PROGRAMMABLE MEMORY SEGMENTS WITHIN A PMOS ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY ARRAY ACHIEVED BY N-WELL SEPARATION AND METHOD THEREFOR	YACH, RANDY L.

Inventor Search Completed: No Records to Display.

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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4	"6260146".pn. "5818274".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 09:49
L2	326	713/172.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 09:54
L3	0	2 and (event adj detect$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 09:50
L4	34574	detect$3 with transition$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 11:02
L5	3	2 and detect$3 with transition$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 09:54
L6	0	5 and ((flip adj2 flop$1) or (bi adj2 stable))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 09:55
L7	1250	713/176.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 11:02
L8	17	7 and detect$3 with transition$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 09:54
L9	0	8 and ((flip adj2 flop$1) or (bi adj2 stable))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 12:22
L10	14	8 and @ad<="20010405"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 11:02
L11	142	713/179.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 11:05
L12	7	11 and detect$3 with transition$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 11:05

L13	7	12 and @ad<="20010405"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 11:05
L14	265	327/217.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 11:07
L15	7	14 and detect$3 with transition$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 11:07
L16	6	15 and @ad<="20010405"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 12:10
L17	318	327/218.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 11:16
L18	8	17 and detect$3 with transition$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 11:16
L19	209	327/225.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 12:09
L20	7	19 and detect$3 with transition$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 12:09
L21	771	375/259.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 12:22
L22	35	21 and detect$3 with transition$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 12:22
L23	28	22 and @ad<="20010405"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 12:22
L24	1418	375/340.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 12:22

L25	115	24 and detect$3 with transition$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 12:22
L26	46	25 and ((flip adj2 flop$1) or (bi adj2 stable))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 12:22
L27	40	26 and @ad<="20010405"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 12:23
L28	15	27 and ((event or error) with detect$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/23 12:23
S1	4	"5087828".pn. "5822386".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/30 09:57
S2	737	375/259.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/30 09:57
S3	458	S2 and ((transmitter$1 and receiver$1) or (modem$1) or (transceiver$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/30 11:56
S5	101	S3 and serial$2 with data	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/30 10:00
S6	40	S5 and detect$3 with ((transition$1 or pulse$1) or (logic adj (state$1 or event$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/30 10:01
S7	37	S6 and @ad<="20010504"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/30 10:02
S8	15	S7 and detect$3 with chang$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/30 10:02
S9	737	375/259.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/30 11:56

S10	430	S9 and ((transmitter$1 and receiver$1) or (transceiver$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/30 11:57
S11	51	S10 and serial adj data	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/30 11:57
S12	37	S11 and (encod$3 and decod$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/30 11:57
S13	33	S12 and @ad<="20010504"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/30 11:58
S14	23	S13 and (controller$1 or computer$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/30 11:58
S15	4	S14 and (detect$3 adj (transition$1 or pulse$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/30 12:00
S16	18058	(serial adj communication$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/30 14:12
S17	11	"370"/366.ccls. and (serial adj communication$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/30 14:13
S18	10	S17 and @ad<="20010405"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/30 14:14